

Notice of References Cited	Application/Control No. 10/019,059	Applicant(s)/Patent Under Reexamination DALTON, DAMIAN	
	Examiner Akash Saxena	Art Unit 2128	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Analysis of an associative array parallel logic simulator; Dalton, D.;Parallel Processing, 1999. Proceedings. 1999 International Workshops on 21-24 Sept. 1999 Page(s):308 - 312
	V	Associative processing and processors; Krikelis, A.; Weems, C.C.; IEEE Computer; Volume 27, Issue 11, Nov. 1994 Page(s):12 - 17
	W	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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